ABSTRACT

A reliable fault-tolerant I/O controller supporting redundant synchronous memories is described. The I/O controller includes multiple I/O control logic units where each I/O control logic unit is in communication with a host server and external peripheral devices. Each I/O control logic unit includes a processor, a memory, and a memory controller. A master I/O control logic unit services I/O transactions from the host server and the external peripheral devices. A slave I/O control logic unit operates in a quiescent state until the master I/O control logic unit experiences a memory failure. At such time, the slave I/O control logic unit resumes operation of the I/O controller. In order to facilitate the switchover from the master I/O control logic unit to the slave I/O control logic unit, the master memory controller performs concurrent memory write operations in both the master and slave memories. The concurrent memory write operations ensure that the memories in both I/O control logic units are in a consistent state in order for the switchover to occur without loss of data.